REMARKS/ARGUMENTS

Claims 1, 6 and 7 are pending in the application, with claims 2-5 having been cancelled. By this amendment, claims 1 and 6 are being amended to improve their form. In addition, Fig. 1B of the drawing is being amended to add a prior art designation, as required in the Office Action. No new matter is involved.

In paragraph 2 which begins on page 2 of the Office Action, claims 1, 6 and 7 are rejected under 35 U.S.C. § 102(b) or 102(e) as being anticipated by admitted prior art set forth on pages 1-3 of the specification. In paragraph 3 on page 4 of the Office Action, claims 1 and 6 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,756,399 of Hajime et al. In paragraph 5 on page 5 of the Office Action, claims 1 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,756,399 of Hajime et al. in view of U.S. Patent 5,800,725 of Kato et al. In paragraph 6 on page 5 of the Office Action, claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hajime or Hajime/Kato and further in view of the admitted prior art. These rejections are respectfully traversed.

In paragraph 7 on page 6 of the Office Action, the requirement is made that Fig. 1B be designated as prior art. In response, applicant is including a replacement sheet which includes such change. Such amendment of the drawing is appropriate and approval is respectfully requested.

In rejecting claims 1, 6 and 7 as anticipated by admitted prior art, the statement is made on page 3 of the Office Action that pages 1-3 of the specification describe a semiconductor wafer. The wafer is obtained by surface-grinding the front or both surfaces of the wafer (claimed flattening one of the surfaces by a surface grinding means); double side polishing of the wafer; and mirror-polishing the front

surface of the wafer. The other surface that is subjected to surface grinding and not to mirror-polishing would have to be the back surface of the wafer.

It is further asserted on page 3 of the Office Action with reference to claim 6 that the admitted prior art doesn't describe that the front surface is without being subjected to surface-grinding. However, the end product would also be the same as the claimed product since it has a mirror-polished front surface as described above and a back surface having micro roughness formed during surface-grinding with the values described in claim 7 of the present invention.

Such statements evidence a misunderstanding of both the prior art described in the specification and the present invention.

As described at line 8 from the bottom of page 1 through line 4 of page 2 of the specification, the prior art comprises a surface-grinding step for surface-grinding the front surface or the both surfaces of the wafer, a double side polishing step for polishing both surfaces of the surface-ground wafer, and a finishing polishing step for mirror-polishing the wafer subjected to the double side polishing. Therefore, the front surface of the wafer is inevitably subjected to surface-grinding. As described at lines 5-25 of page 2, such prior art structure suffers from the problem that grinding striations remain on the front surface of the wafer even after the wafer is polished or mirror-polished (as shown in Fig. 1B(g); grinding striations 4 remain on the front surface of the end product). On the contrary, there may be the case where the back surface is subjected to surface-grinding or not. Moreover, there may be the case where the back surface is mirror-polished or not. Namely, the surface-grinding and polishing of the back surface are optional. When the back side of the wafer is also mirror-polished, as described from line 2 from the bottom of page 2 through line 6 of page 3 of the patent specification, because flatness on the back surface is too good, which may easily cause problems in a device process, such

as indistinguishability of the front surface from the back surface, necessity of re-adjustment of sensing sensitivity, difficulty of chucking and releasing the water, and liabilities in a conveying line such as contamination. In contrast, independent claims 1 and 6 distinguish the present invention patentably over such prior art. As amended herein, claims 1 and 6 read as follows:

> 1. A semiconductor wafer obtained, at least, by removing a mechanical damage layer by etching both of opposite front and back surfaces of the wafer, flattening the back surface by a surface-grinding means to the exclusion of the front surface of the wafer, polishing both of the front and back surfaces, and then subjecting the front surface of the wafer to a finishing mirror-polishing when defining the surface subjected to surface-grinding as the back surface of the wafer.
>
> 6. A semiconductor wafer, wherein the wafer has opposite front and back surfaces, the front surface is subjected to a finishing mirror-polishing without being subjected to surface-grinding, the back surface is subjected to surface-grinding, and micro roughness formed during surface-grinding remains on the back surface.

Thus, in the present invention, the front surface of the wafer is not subjected to surface-grinding without exception, but the back surface of the wafer is inevitably subjected to surface-grinding. As defined in claim 1, the back surface is surface ground to the exclusion of the front surface with the surface-ground surface side of the wafer regarded as the back surface, and the front surface is mirror-polished. Therefore, because the front surface of the wafer is not subjected to surface-grinding although the back surface of the wafer is subjected to surface-grinding, grinding striations remain on the back surface. As shown in Fig. 1A(g), in the case of the

present invention, the end product has no grinding striations on the front surface side but has grinding striations 4 on the back surface side.

Therefore, the present invention differs from the admitted prior art in that the front surface of the wafer is not subjected to surface-grinding and thus grinding striations do not remain thereon. The present invention also differs from the admitted prior art in that although the back surface of the wafer of the present invention is subjected to surface-grinding but not mirror-polished, the prior art is not limited thereto.

Thus, the invention as defined in claim 1 patentably distinguishes from the admitted prior art in the specification. The wafer according to the present invention can realize the beneficial affect that because grinding striations do not exist on the front surface but remain on the back surface, it is easy to distinguish the front surface from the back surface (see page 4 of the specification, for example). Therefore, claim 1 is submitted to clearly distinguish patentably over the admitted prior art. Similar comments apply to claim 6 as amended herein. Claim 7 depends from and contains all of the limitations of the claim 6 so as to also distinguish patentably over the admitted prior art.

In rejecting claims 1 and 6 as anticipated by the Hajime et al. '399 reference, it is stated in the Office Action that such reference teaches a semiconductor wafer which has two sides. It is said that this would read on the claimed wafer with opposite front and back surfaces. Also, the wafer has micro roughness remaining on the back surface because the reference also teaches that either surface can be subjected to surface grinding. According to the Office Action, this would also read on the front side without being subjected to surface-grinding.

However, the corresponding portions of Hajime et al. as referred to in the Office Action describe virtually the same technique as is described on pages 1-3 of

the present specification. According to such technique, after one surface or both surfaces of the wafer are subjected to surface-grinding, the one surface or both surfaces of the surface-ground wafer is polished. This is made clear in the claim of Hajime et al. It is also clear from the wording "polishing the one side or the both sides" (it is also mentioned in the corresponding Japanese patent application).

Therefore, it can be concluded that the front surface of the wafer to be polished is inevitably subjected to surface-grinding. Therefore, as previously mentioned, grinding striations remain on the front surface of the polished wafer. On the contrary, the back surface of the wafer may be subjected to surface-grinding or not. Moreover, the back surface may be polished or not in the subsequent step. Namely, the surface-grinding or polishing on the back surface is arbitrary.

On the contrary, and as previously mentioned, in independent claims 1 and 6, the front surface of the wafer is not subjected to surface-grinding without exception, but the back surface is inevitably subjected to surface-grinding. Therefore, because the front surface of the wafer in accordance with the present invention is not subjected to surface-grinding, but mirror-polished, grinding striations do not exist thereon, and because the back surface is subjected to surface-grinding, grinding striations remain thereon.

Therefore, the present invention differs from Hajime et al. in that the front surface of the wafer is not subjected to surface-grinding. In other words, grinding striations do not remain thereon. The present invention also differs from Hajime et al. in that although the back surface of the wafer in accordance with the present invention is subjected to surface-grinding but not mirror-polished, Hajime et al. is not limited thereto.

Therefore, claims 1 and 6 are submitted to clearly distinguish patentably over Hajime et al.

In connection with the rejection of claims 1 and 6 as unpatentable over Hajime et al. '399 in view of U.S. Patent 5,800,725 of Kato et al., it is stated in the Office Action that Hajime describes the product produced by a different method in which the front surface is subjected to a mirror-polishing step. Kato teaches a method for forming a semiconductor wafer where it is described that the front surface is subjected to a mirror-polishing step. It would have been obvious for one of ordinary skill in the art to add a mirror-polishing step in light of Kato in order to have a final mirror surface of the wafer.

However, and as previously mentioned, Hajime et al. only describes that the front surface of the wafer to be polished is inevitably subjected to surface-grinding, and grinding striations remain on the front surface of the polished wafer. Such reference does not disclose the wafer as in the case of the present invention to which the front surface is not subjected to surface-grinding without exception, but the back surface is inevitably subjected to surface-grinding.

Therefore, the present invention is not made obvious by Hajime et al. in combination with Kato et al., which only describes a finished mirror-polishing. Claims 1 and 6 are submitted to clearly distinguish patentably over the attempted combination of Hajime and Kato.

Claim 7, which was rejected as unpatentable over Hajime or Hajime/Kato in view of the admitted prior art, depends from and contains all of the limitations of claim 6. Therefore, claim 7 is also submitted to clearly distinguish patentably over the prior art.

In conclusion, claims 1, 6 and 7 are submitted to clearly distinguish patentably over the prior art for the reasons discussed herein. Accordingly, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: September 22, 2003

By: _____
John P. Scherlacher
Registration No. 23,009
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701